



H55H-I V1.0A

SCHEMATICS TABLE:

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REVISION HISTORY:

Rev	Date	Notes
A	2009/10/15	First release
1.0	2009/12/15	1. modify EC18 to small CAP 2. swap EC26 and EC27, change EC26 to lower CAP 3. modify H_VTTPWRGD 4. remove C36, C40 5. add LPC_DEBUG header 6. keep SPI ROM far away L8 7. SPI_DEBUG signal add damping 8. change Memory DIMM2 SMB address 9. add VAXG switching MOS damping 10. V_3P3_DAC_FB add 10U CAP 11. add CPU SKTOCC 12. Super I/O pin14 remove 10U CAP, add 22n CAP(follow ITE)
1.0A	2010/01/19	1. SWAP SU11 pin3.4, fix front USB loss power in S3 state

IMPORTANT NOTES ABOUT THIS SCHEMATIC

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

1) DESIGN NOTES in grey are information notes.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

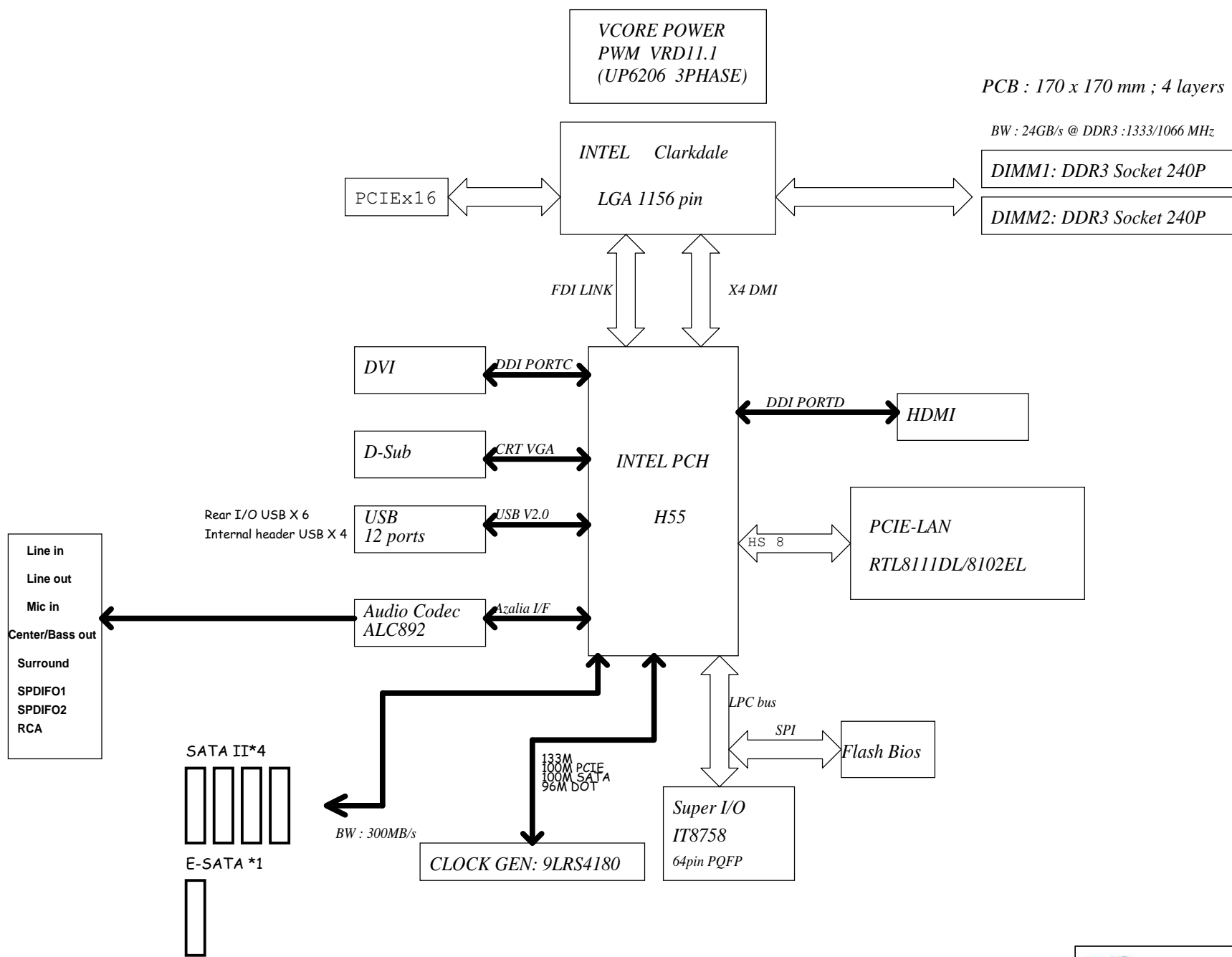
2) DESIGN NOTES in yellow are notes of caution.

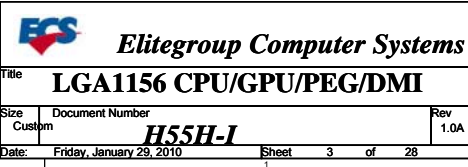


3) DESIGN NOTES in red are critical, and must be understood and followed.

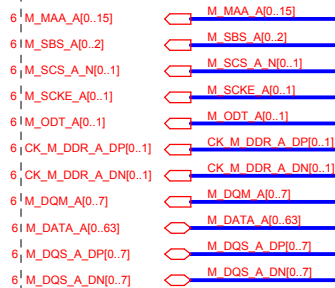
PCB STACK: L1:TOP
L2:POWER
L3:IN1
L4:IN2
L5:GND
L6:BOTTOM

Elitegroup Computer Systems		
Title Cover Page		
Size Custom	Document Number H55H-I	Rev 1.0A
Date: Friday, January 29, 2010 Sheet 1 of 28		

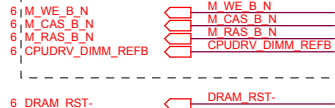
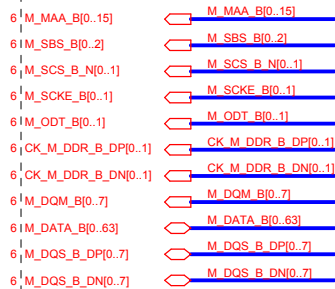




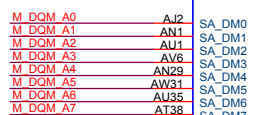
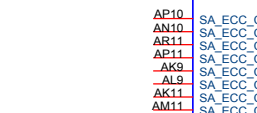
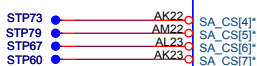
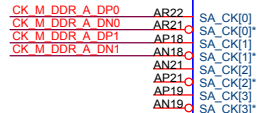
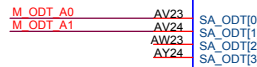
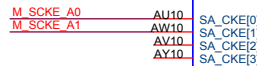
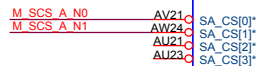
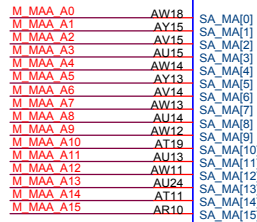
CHANNEL A



CHANNEL B



CPUA

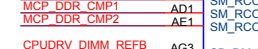
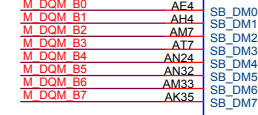
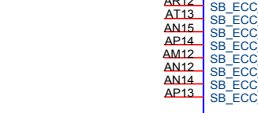
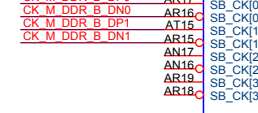
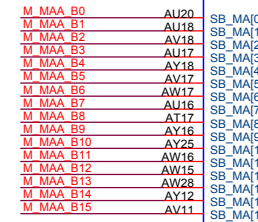


DDR_A

LGA1156_H

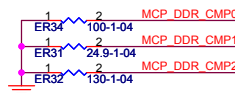
1 OF 7

CPUB



DDR_B

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Elitegroup Computer Systems

Title

LGA1156 DDR3 MEMORY

Size

Document Number

Rev

1.0A

Date:

Friday, January 29, 2010

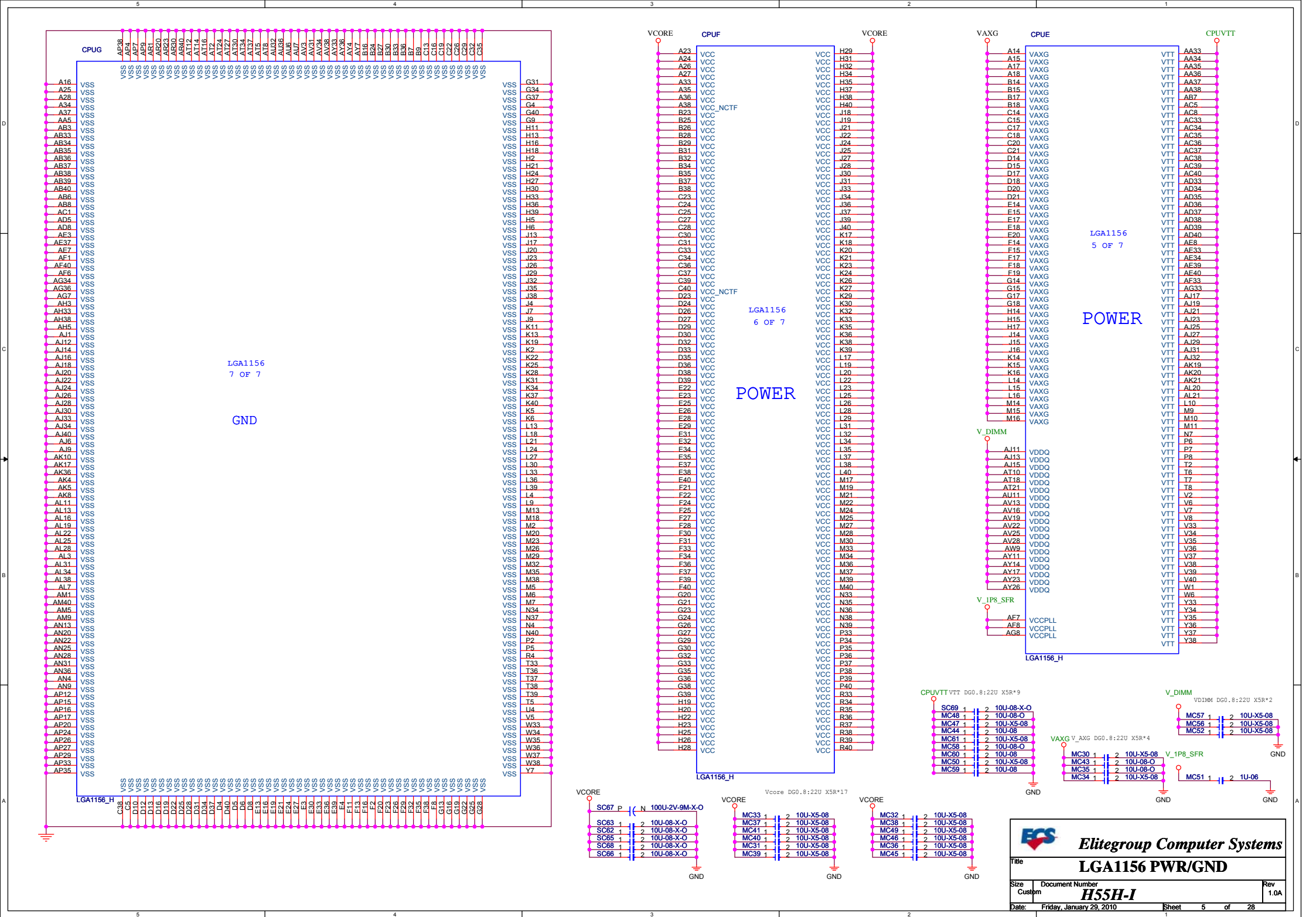
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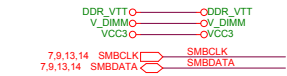
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28

H55H-I



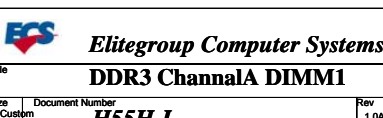
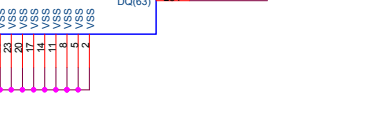
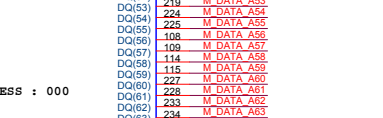
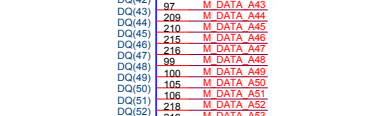
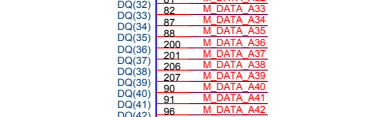
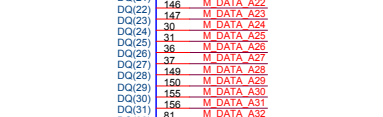
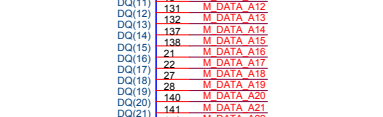
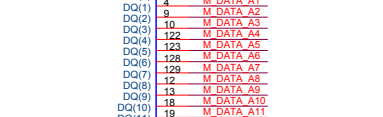
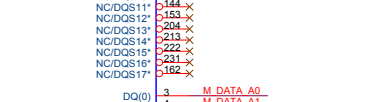
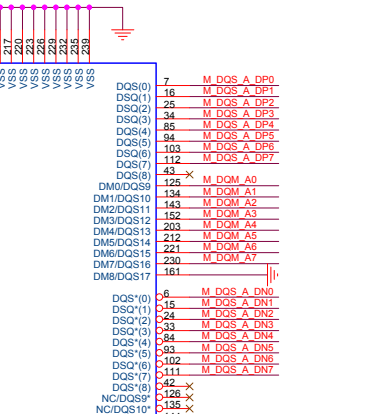
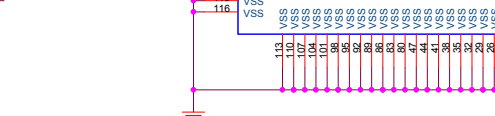
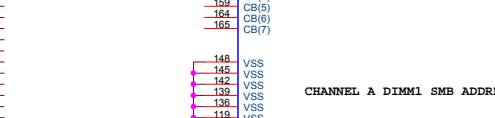
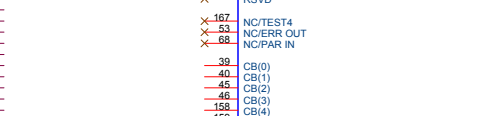
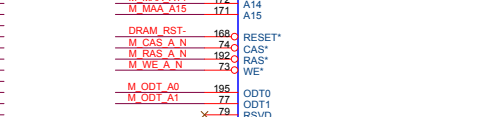
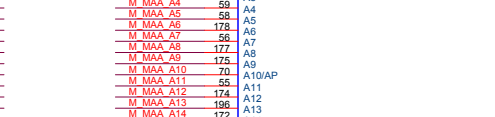
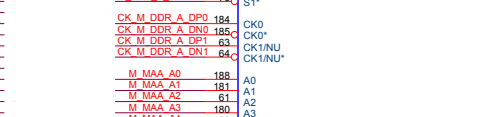
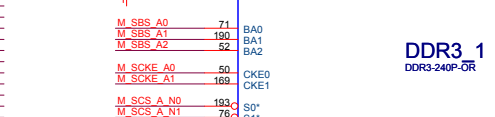
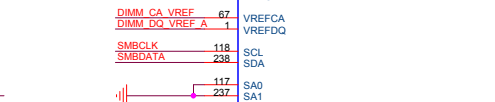
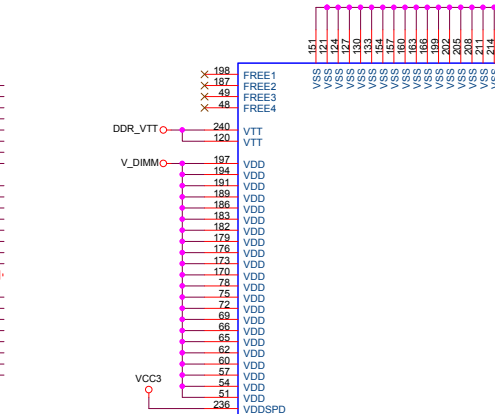
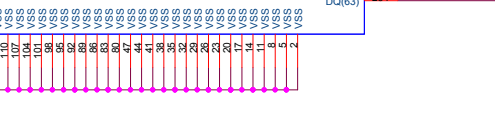
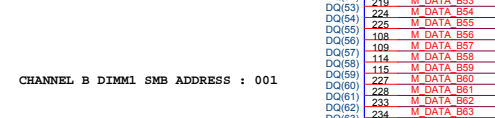
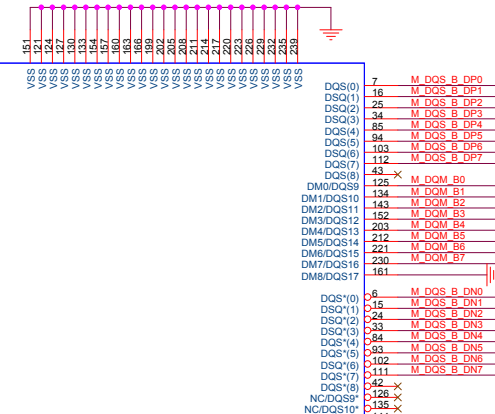
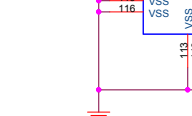
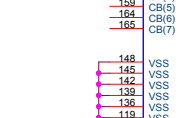
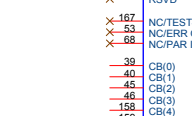
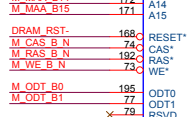
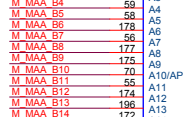
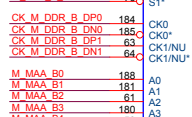
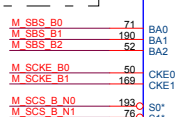
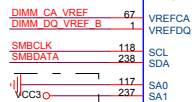
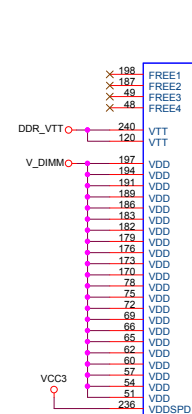
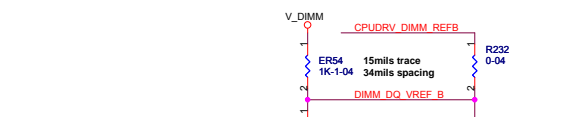
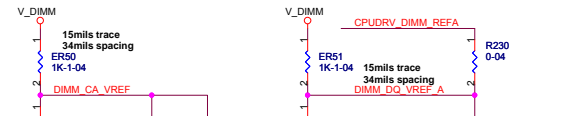
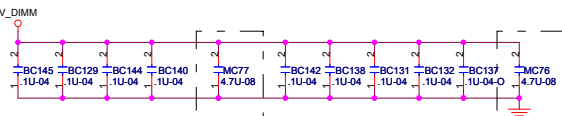
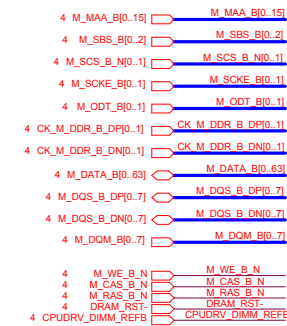
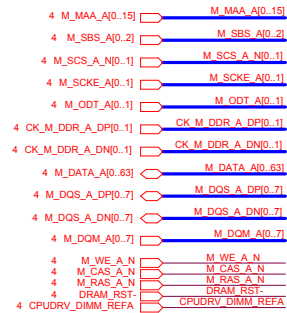
External Connection



COMMON

ChannelA

ChannelB



Elitegroup Computer Systems

DDR3 ChannelA DIMM1

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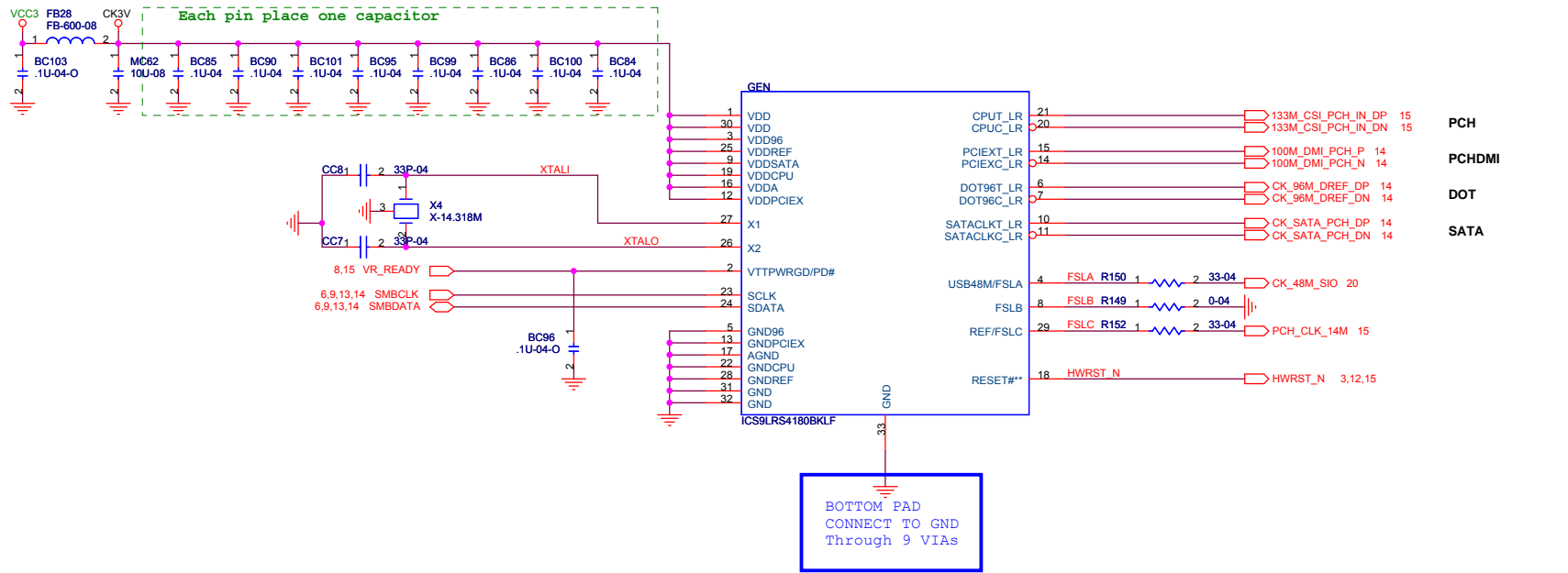
Document Number: H55H-I

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Date: Friday, January 26, 2010

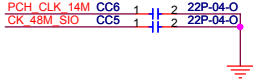
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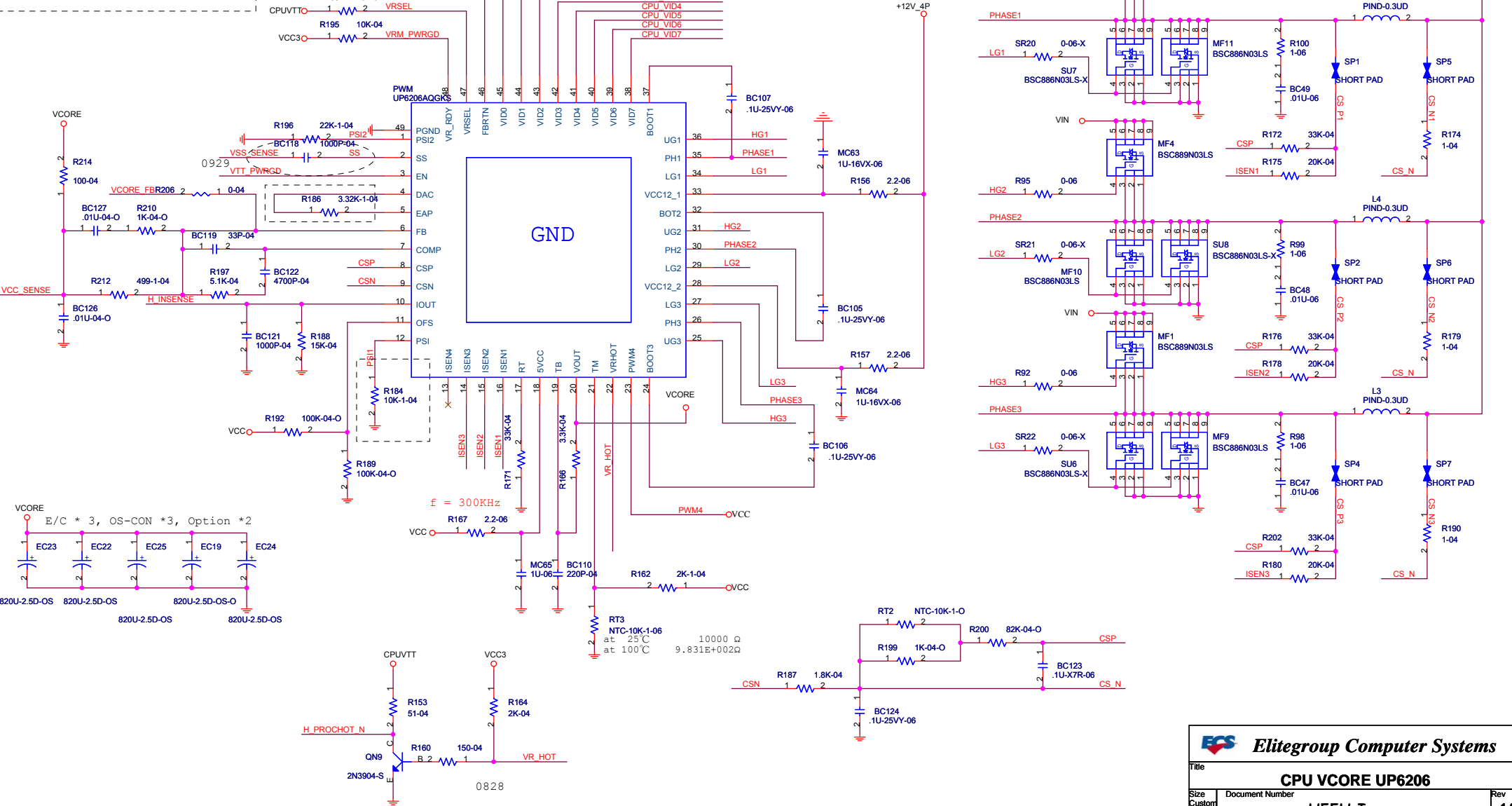
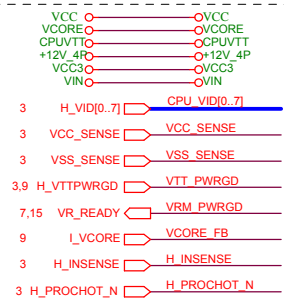


FSLC,FSLB,FSLA = 001, CPU_CLK = 133MHz

FSLC (B0b2)	FSLB (B0b1)	FSLA (B0b0)	CPU MHz	PCIE MHz	SATA MHz	DOT96 MHz
0	0	1	133.33	100	100	96.00
1	0	1	100.00	100	100	96.00



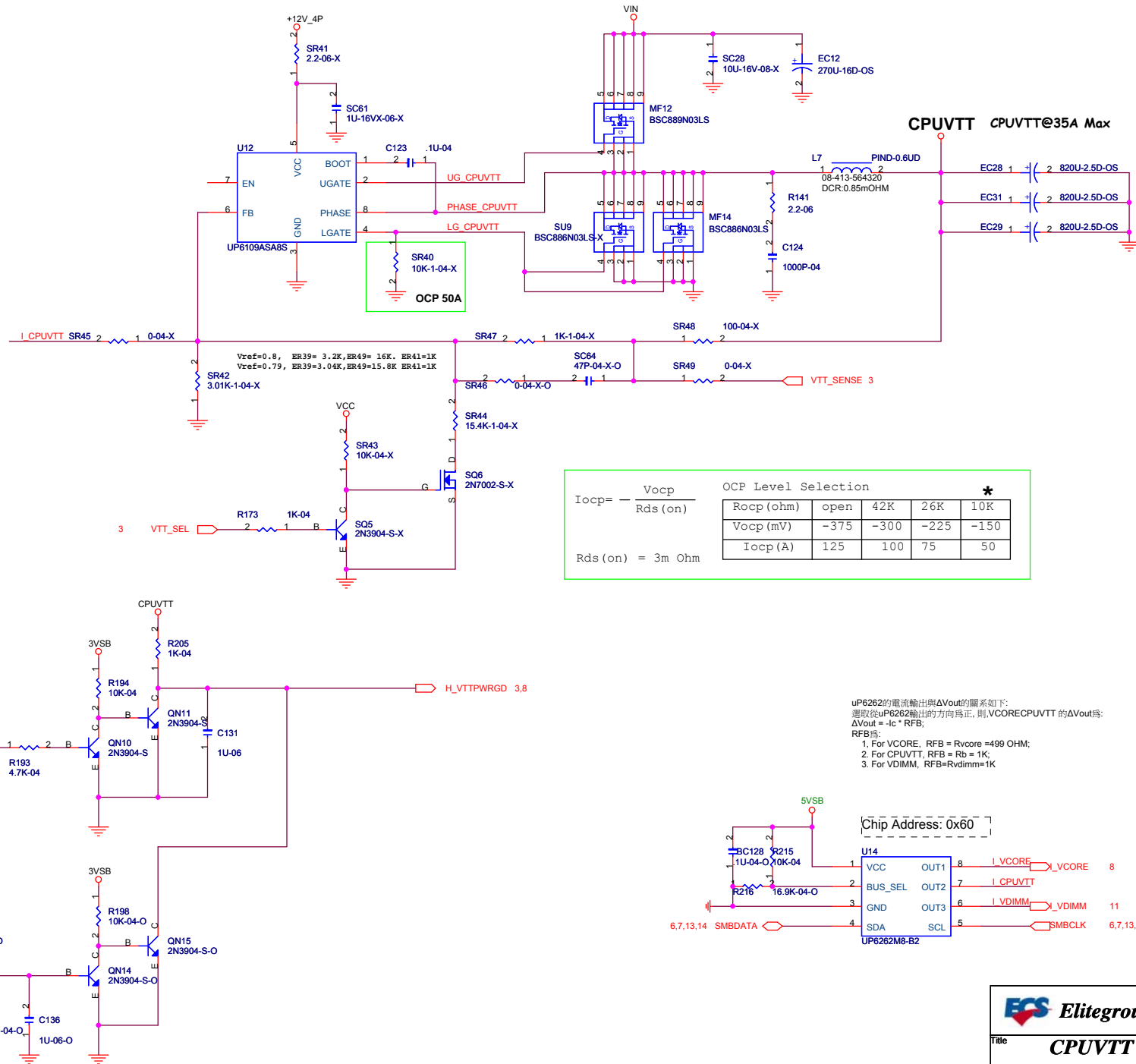
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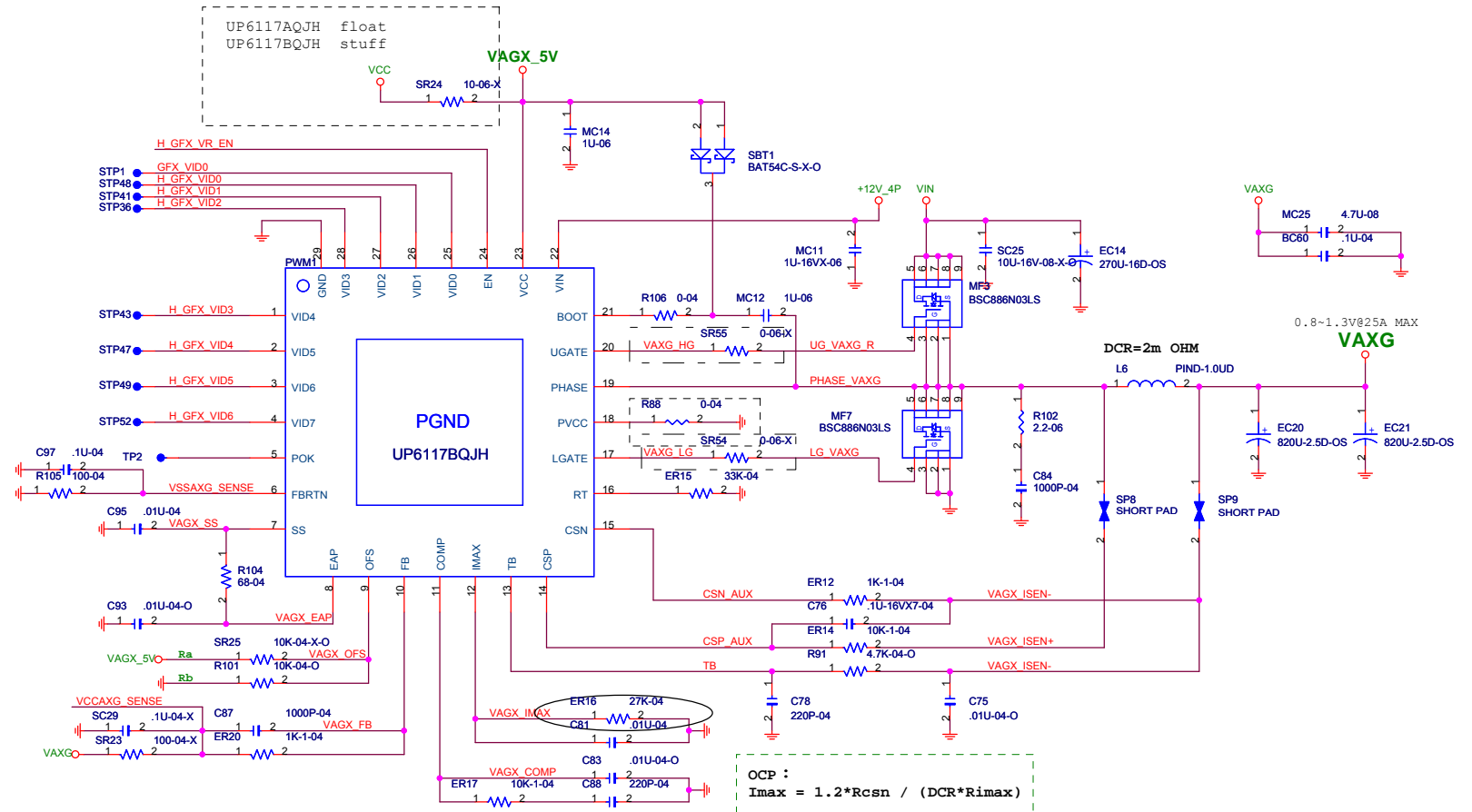
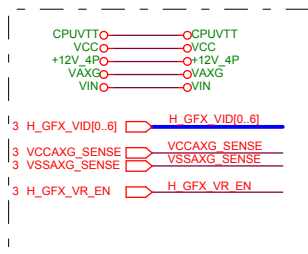


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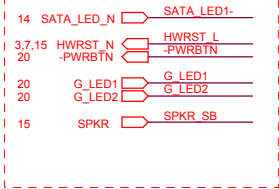
VTT_SEL	CPUVTT
1	1.05V
0	1.10V



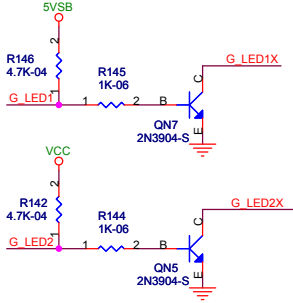
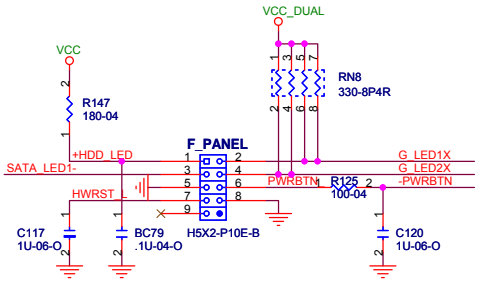
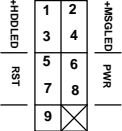


FRONT PANEL

External Connection



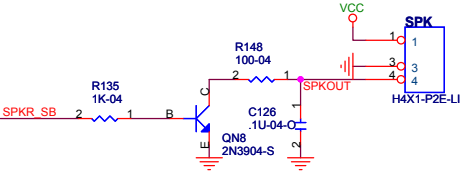
F. PANEL



	S0	S1	S3	S4	S5
G_LED1	L	B	B	L	L
G_LED2	H	H	L	L	L
	G	GB	YB	OFF	OFF

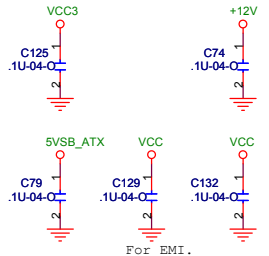
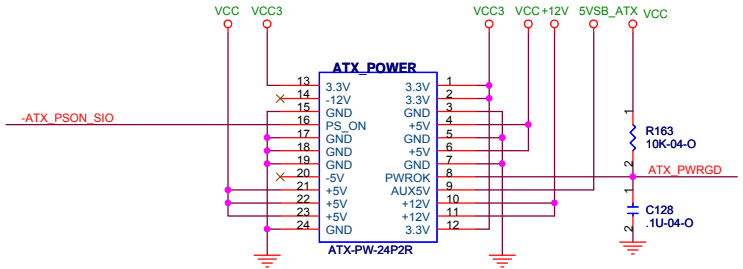
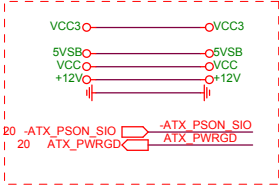
B: Blinking

BUZZER SPK Colay



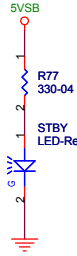
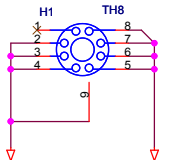
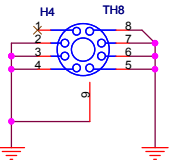
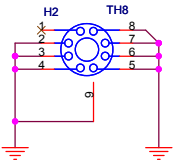
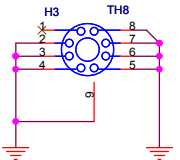
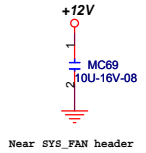
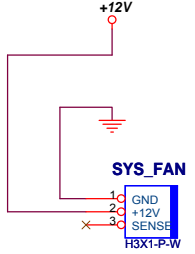
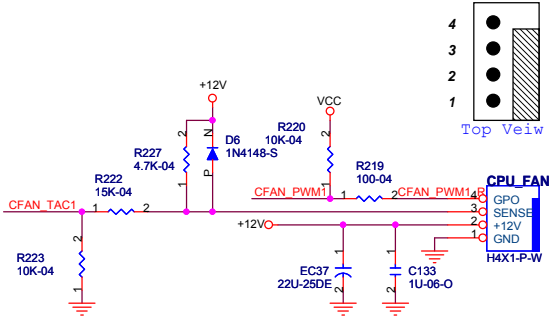
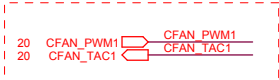
POWER CONNECTOR

External Connection



FAN

External Connection



Title: **Front Panel,FAN,PowerConn**

Size: Custom

Date: Friday, January 29, 2010

Document Number: **H55H-I**

Rev: 1.0A

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3VSB
VCC3
+12V

3 EXP_A_RX_DP[0..15]
3 EXP_A_RX_DN[0..15]
3 EXP_A_TX_DP[0..15]
3 EXP_A_TX_DN[0..15]

EXP_A_RX_DP[0..15]
EXP_A_RX_DN[0..15]
EXP_A_TX_DP[0..15]
EXP_A_TX_DN[0..15]

15 CK_PE_100M_16P_A_DN
15 CK_PE_100M_16P_A_DP

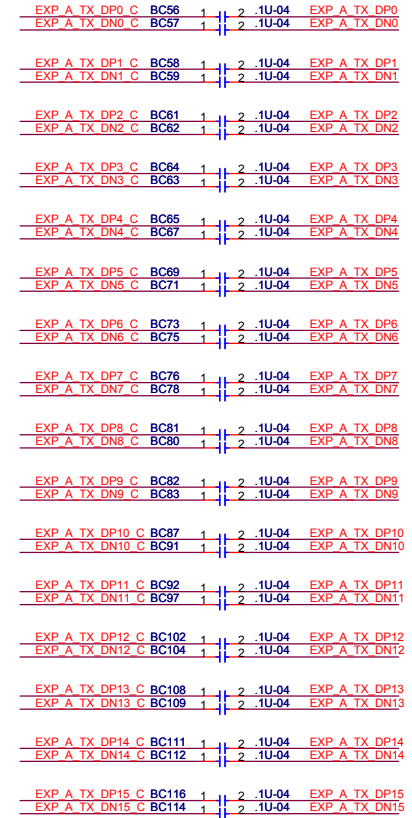
CK_PE_100M_16P_A_DN
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6,7,9,14 SMBCLK
6,7,9,14 SMBDATA

SMBCLK
SMBDATA

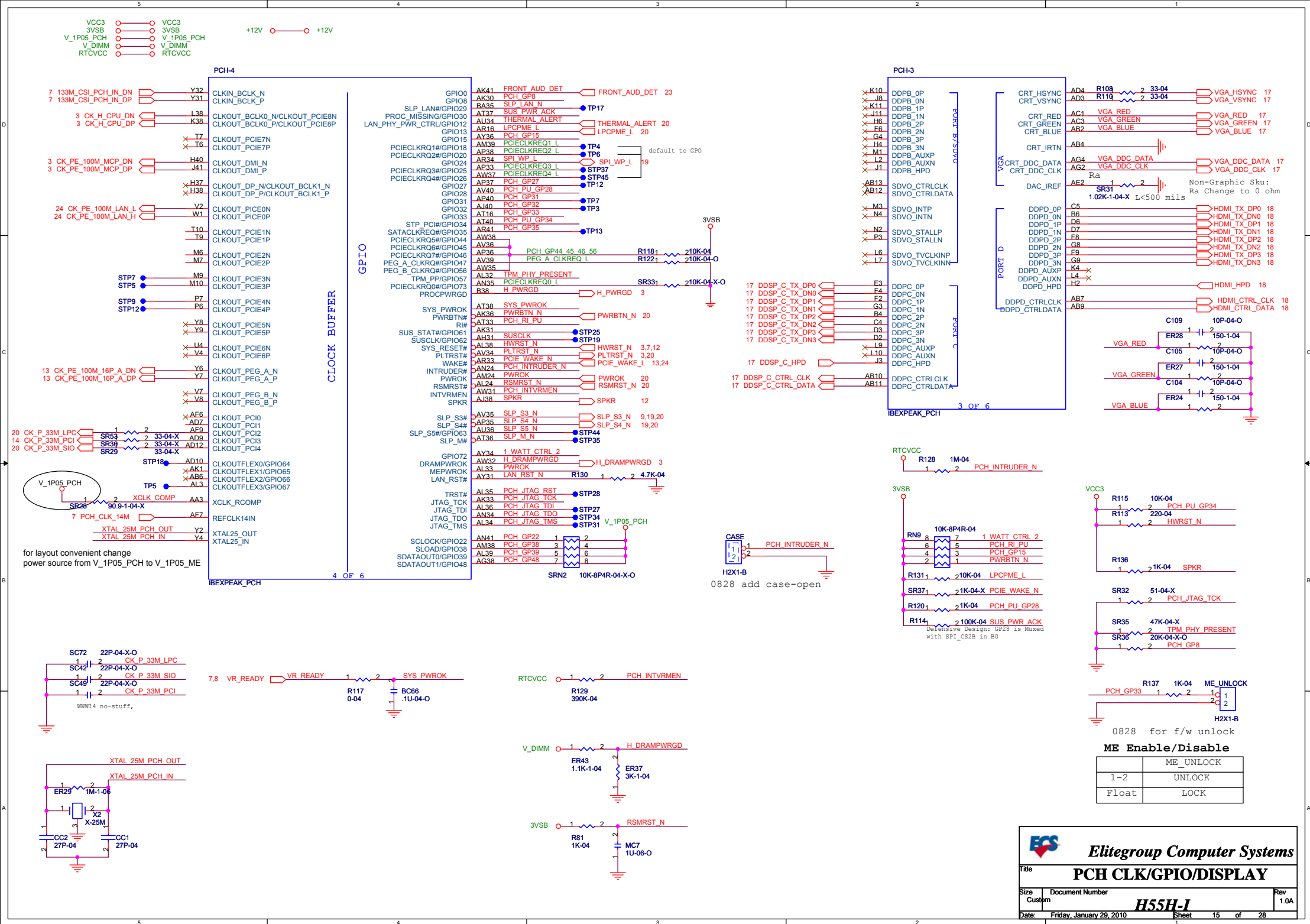
20 -PCI_RSTY
15,24 PCIE_WAKE_L

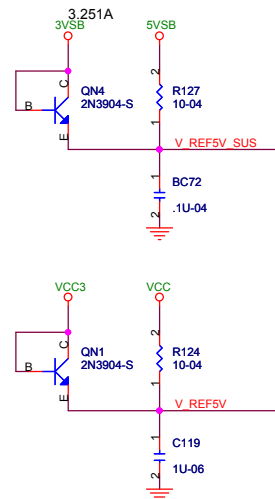
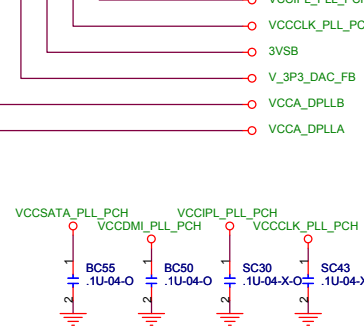
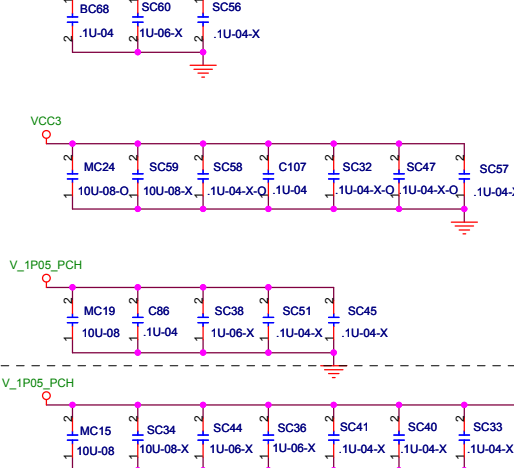
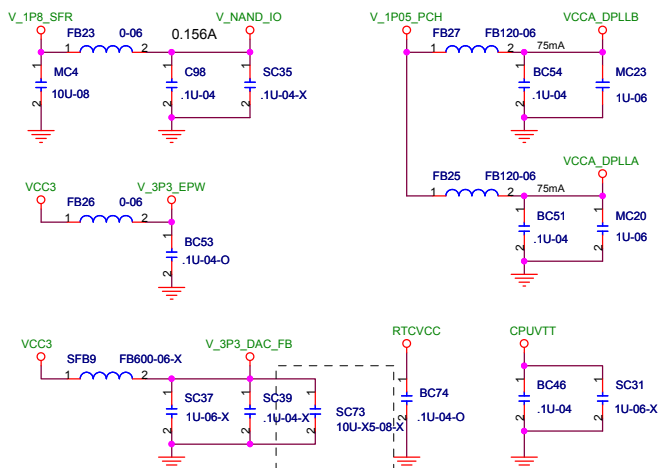
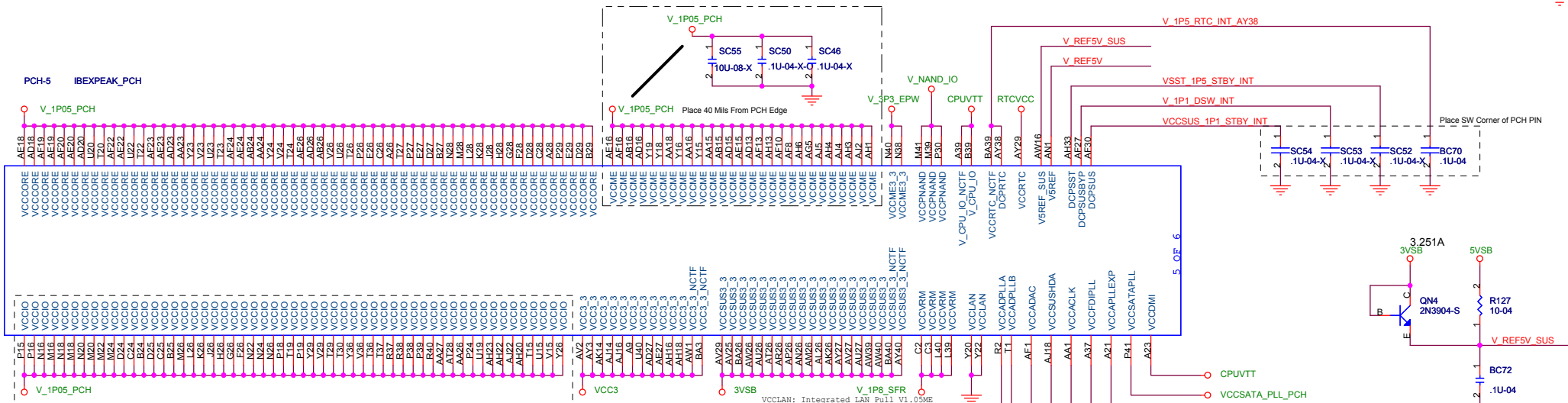
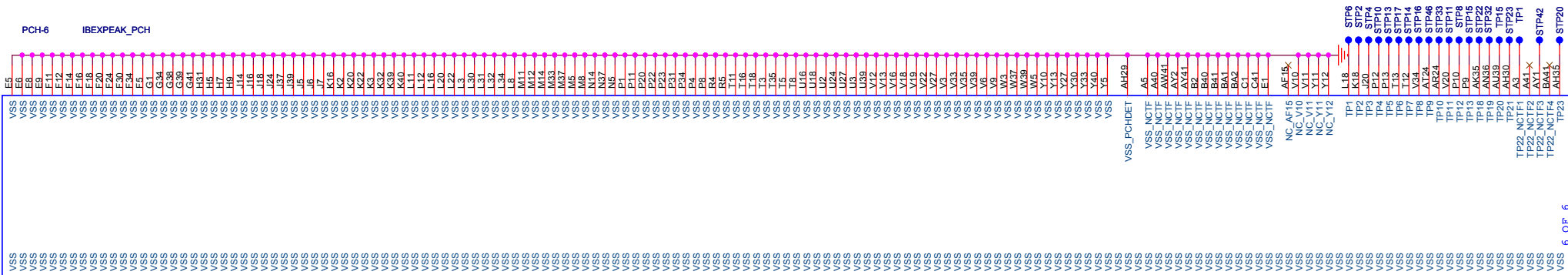
PCI_RSTY
PCIE_WAKE_L



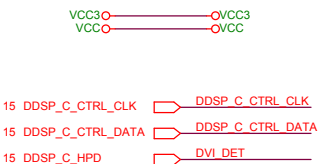
Three circuit diagrams are shown, each representing a different power supply connection:

- 3VSB:** A circuit with a 3VSB supply, a BC52 transistor, and a 1U-04 capacitor.
- VCC3:** A circuit with a VCC3 supply, a MC22 transistor, a 10U-08-O capacitor, and an EC18 220U-16DE capacitor.
- +12V:** A circuit with a +12V supply, a BC39 transistor, a 1U-04 capacitor, and an EC13 470U-16DE capacitor.

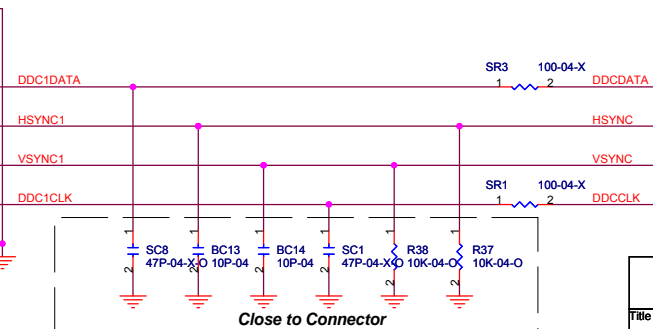
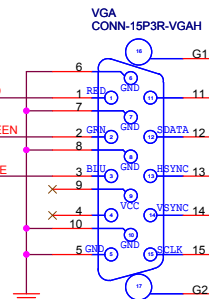
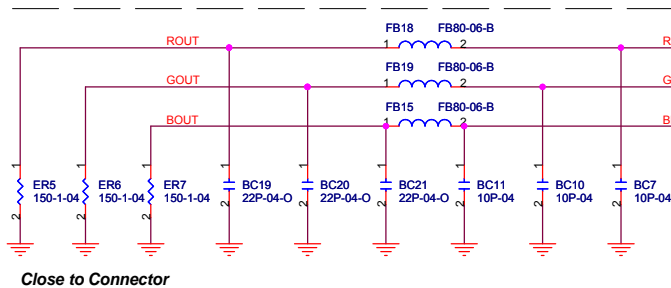
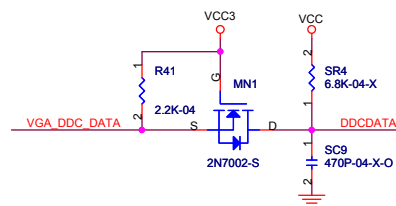
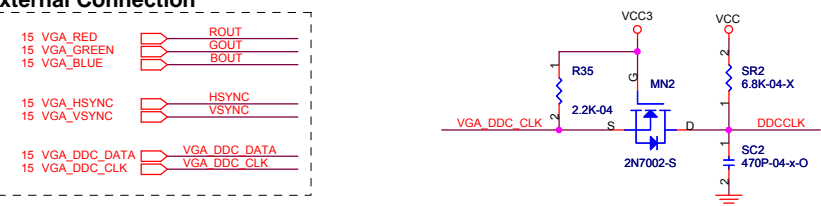
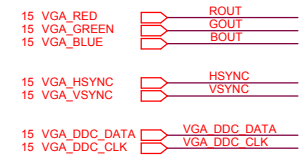




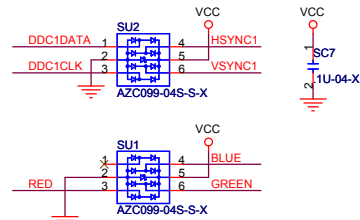
External Connection



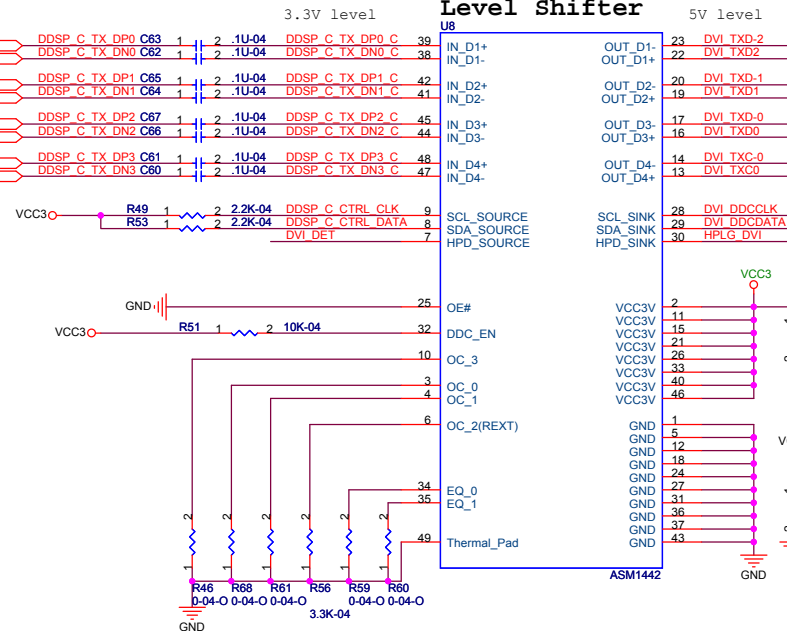
External Connection



ESD

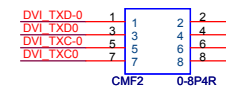
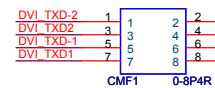
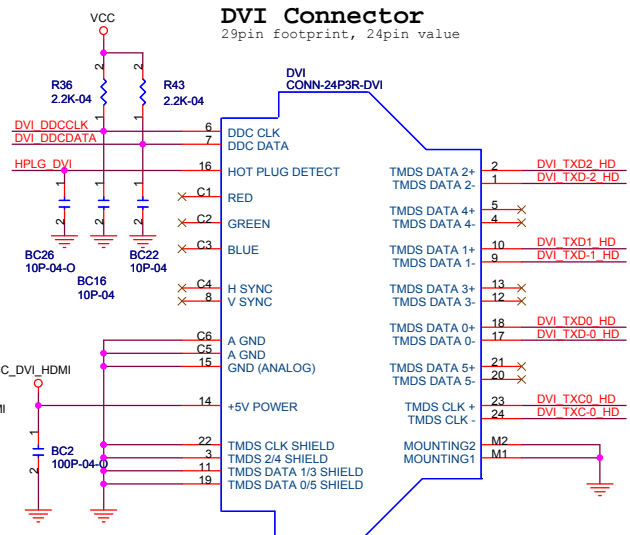


Level Shifter



DVI Connector

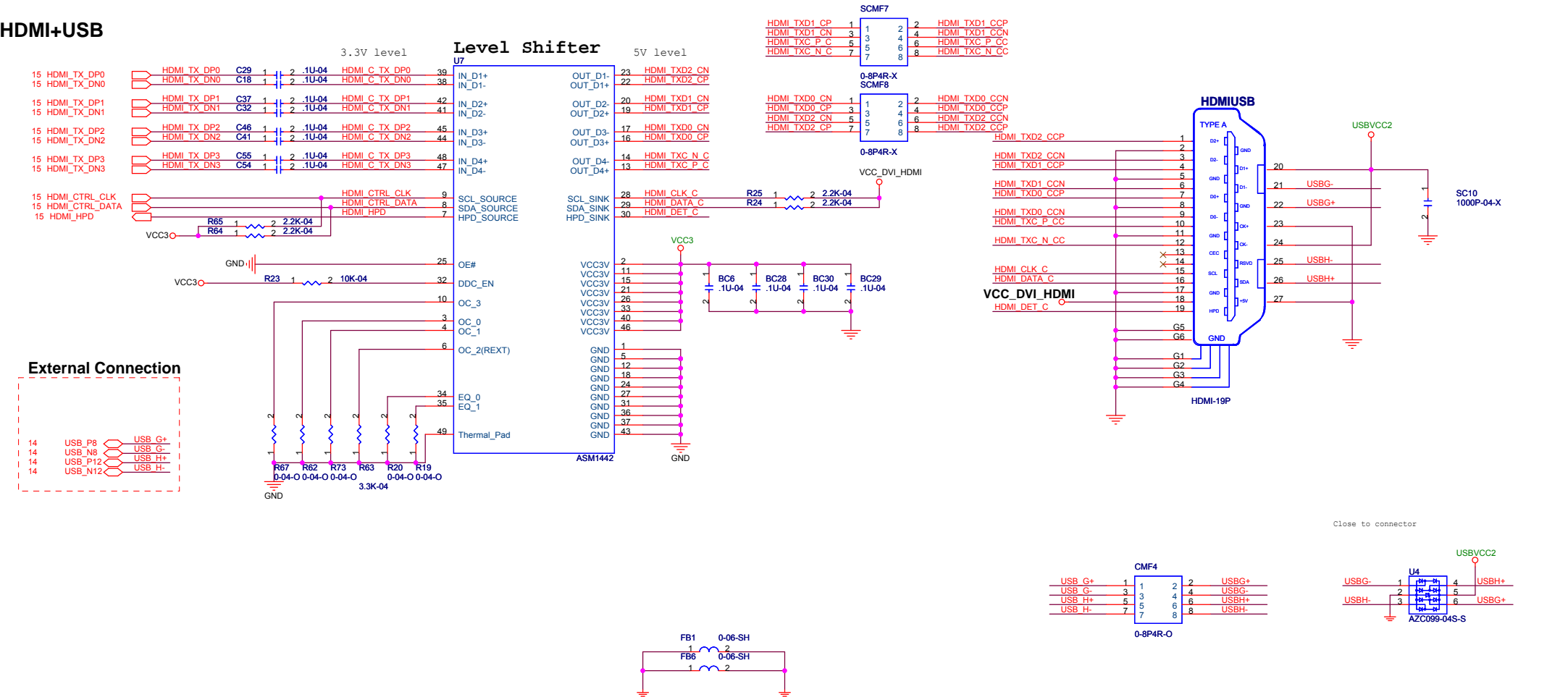
29pin footprint, 24pin value



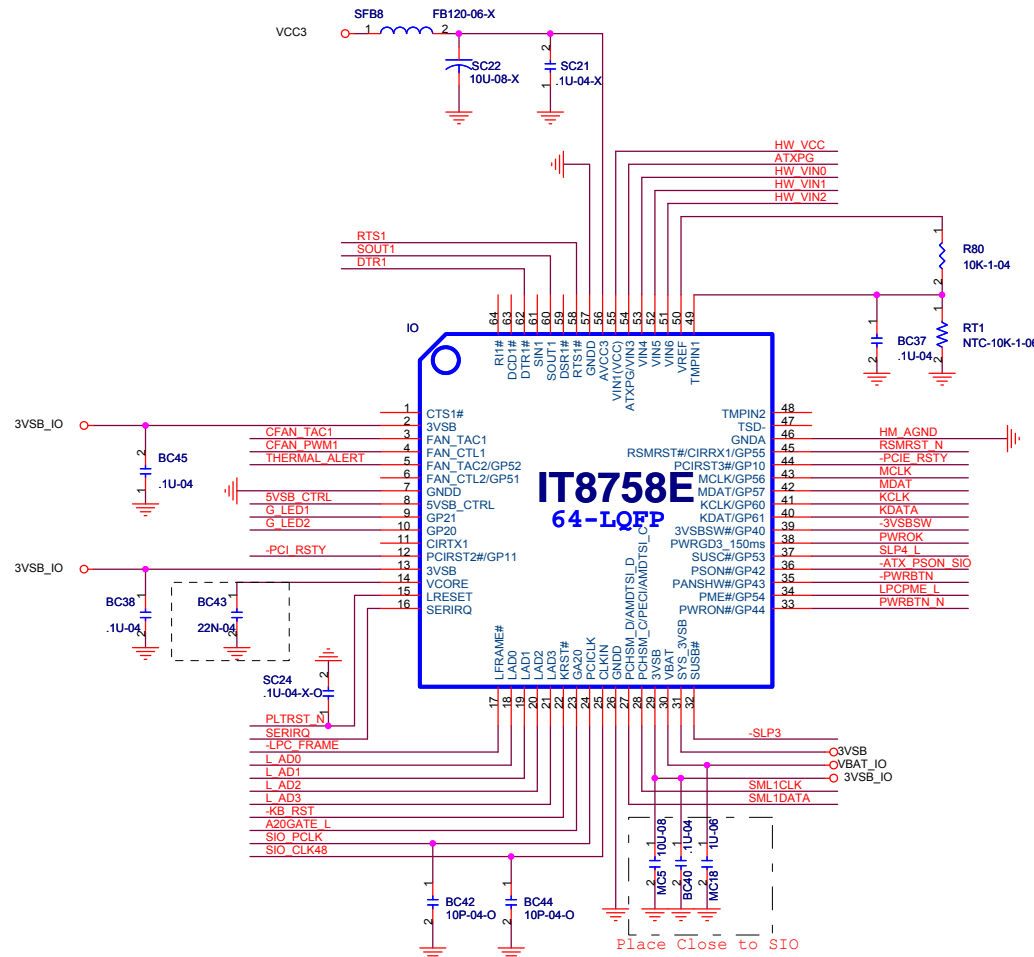
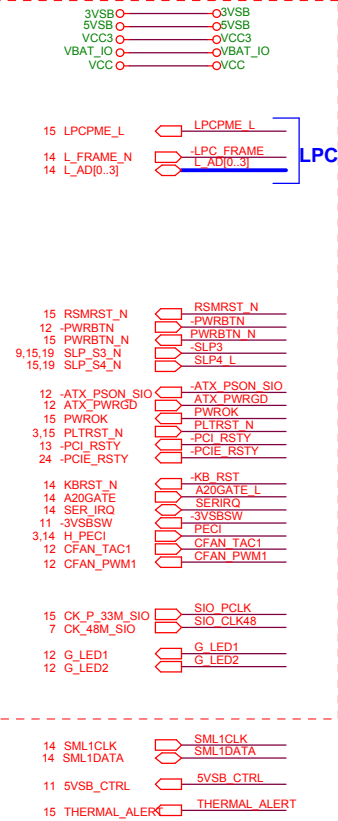
Elitegroup Computer Systems

Title	DVI, RGB		
Size	Document Number	Rev	
Custom	H55H-I	1.0A	
Date:	Friday, January 29, 2010	Sheet	17 of 28

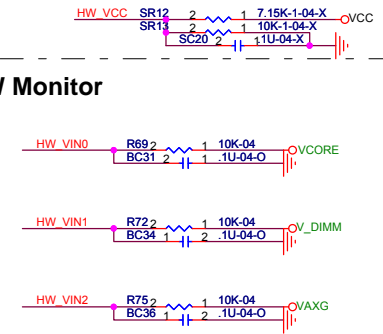
HDMI+USB



External Connection

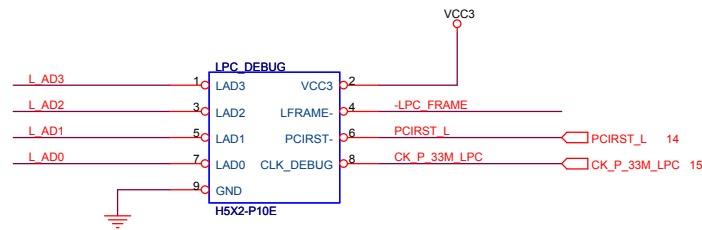
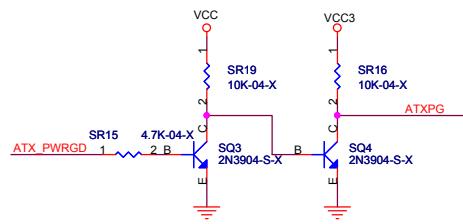
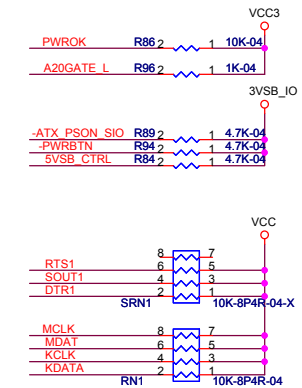


H/W Monitor

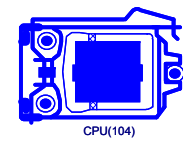
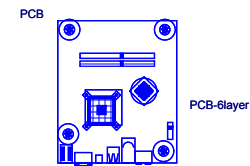
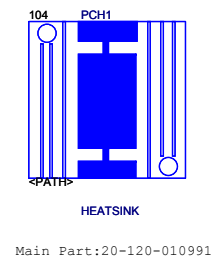
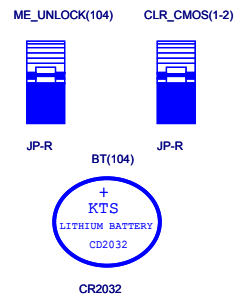


LPC Pull-ups

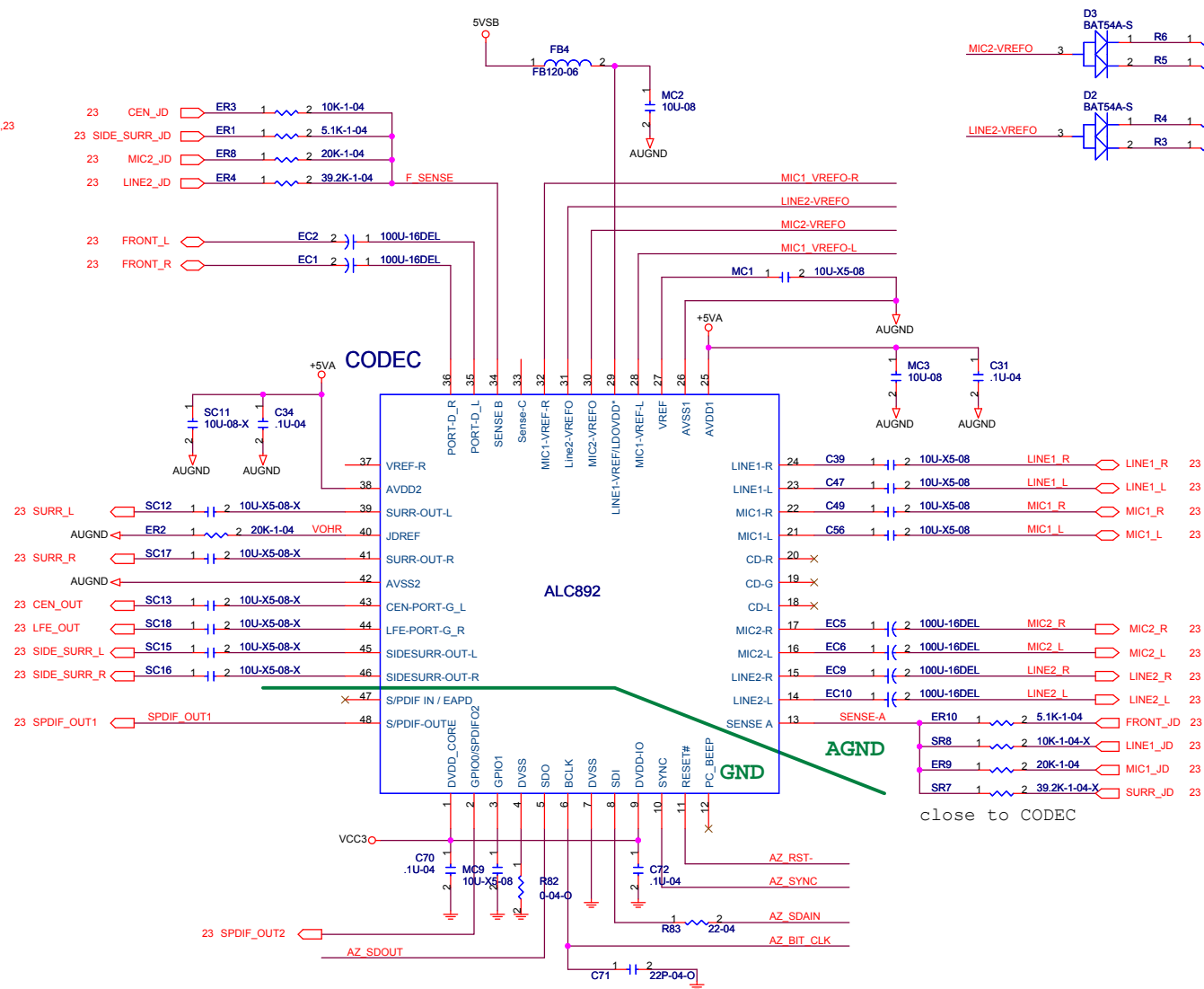
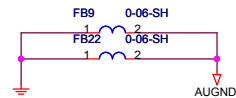
Note:
Most pull-ups are provided



1080 : trace width 4 mil 50 ohm
Trace Length 3150 mils
Spacing: 1.clearance to itself 50/4/50(S:W:S)
2.clearance to other signal 3W



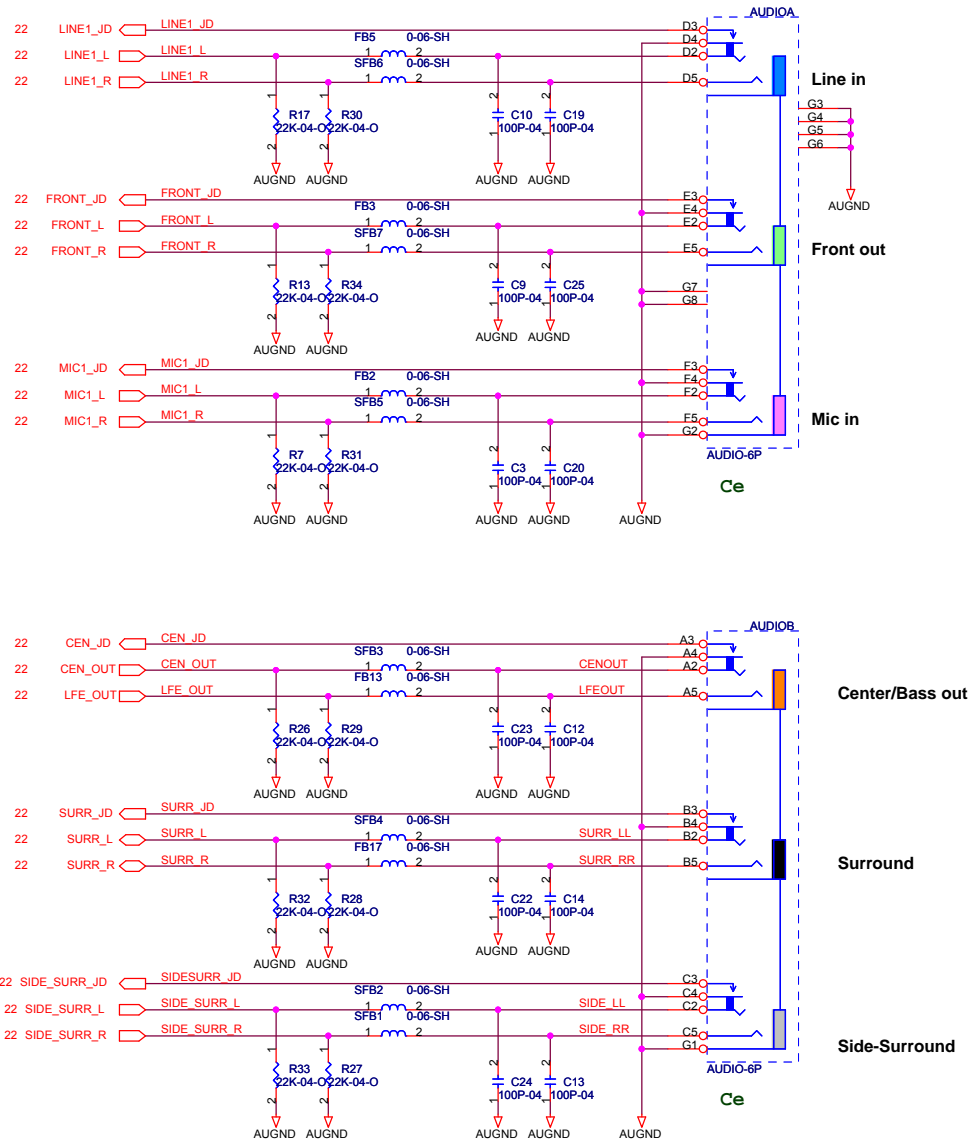
Pin configuration diagram for the HDA codec. The diagram shows a 16-pin connector with pins 14 and 15. Pin 14 is connected to HDA_RST_N, HDA_BCLK, HDA_SYNC, HDA_SDINO, and HDA_SDO. Pin 15 is connected to FRONT_AUD_DET. The diagram also shows power connections: 5VSB to VCC and +12V to VCC3. The AGND and AUGND pins are connected to ground.



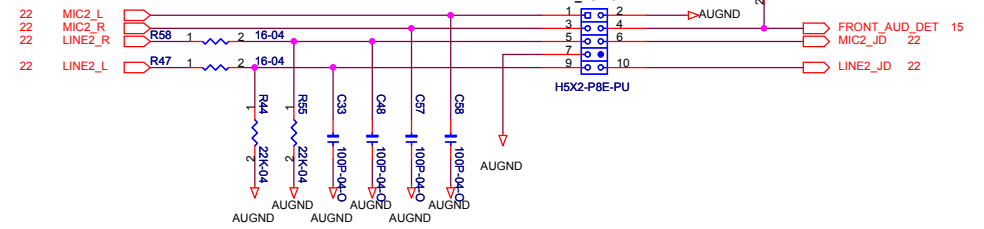
The schematic diagram illustrates the input stage of the 68000 microprocessor, featuring three comparators and their associated resistors and output labels.

- Comparator R40:** The input MIC1_VREFO-R is connected to pin 1. The output of the comparator is connected to pin 2, which is also connected to a 2.2K-04 resistor. The output label is MIC1_R.
- Comparator R39:** The input MIC1_VREFO-L is connected to pin 1. The output of the comparator is connected to pin 2, which is also connected to a 2.2K-04 resistor. The output label is MIC1_L.
- Comparator D3 (BAT54A-S):** The input MIC2_VREFO is connected to pin 3. The output of the comparator is connected to pin 1, which is also connected to a 4.7K-04 resistor. The output label is MIC2_R.
- Comparator D2 (BAT54A-S):** The input LINE2_VREFO is connected to pin 3. The output of the comparator is connected to pin 2, which is also connected to a 4.7K-04 resistor. The output label is LINE2_L.

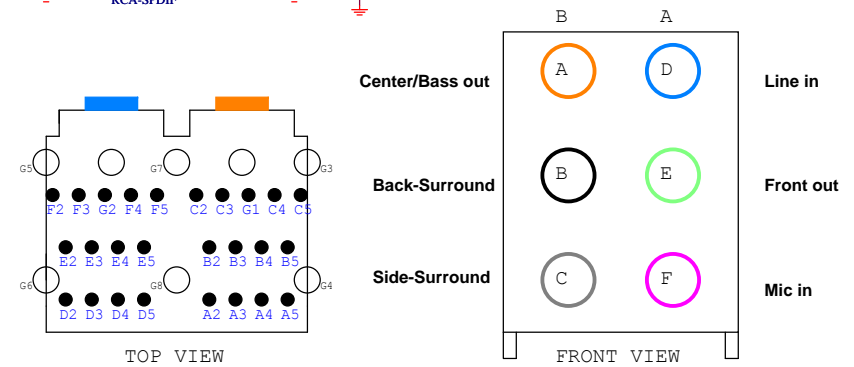
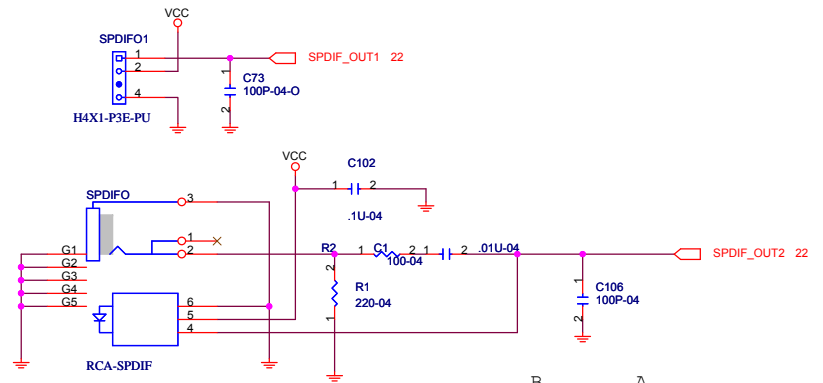
Rear Panel Onboard Analog I/O



FRONT-AUDIO



SPDIF1-OUT



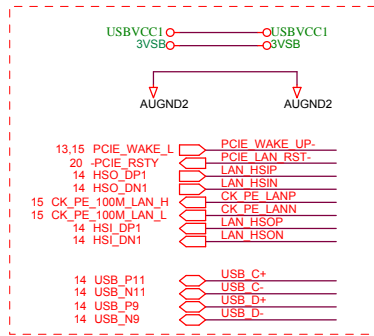
ECS Elitegroup Computer Systems

Title: **Audio Connector**

Size: Custom Document Number: **H55H-I** Rev: 1.0A

Date: Friday, January 29, 2010 Sheet: 23 of 28

External Connection



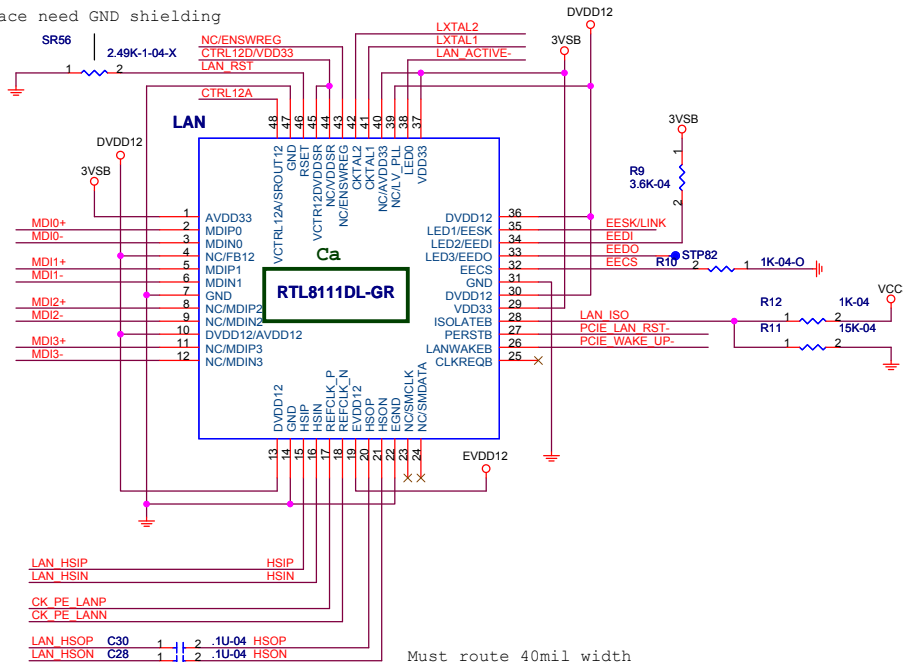
新手提醒:

LAN_HSOP/N請接到SB的PCIE RX端

LAN_HSI/N請接到SB的PCIE TX端

LAN_HSI/N在SB的PCIE TX端要記得放AC coupling cap

RSET電阻需close to LAN
Trace need GND shielding



Must route 40mil width
La_C4 place at pin44 with 200mil distance



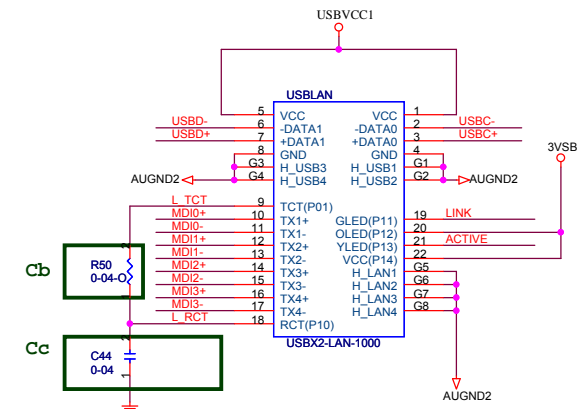
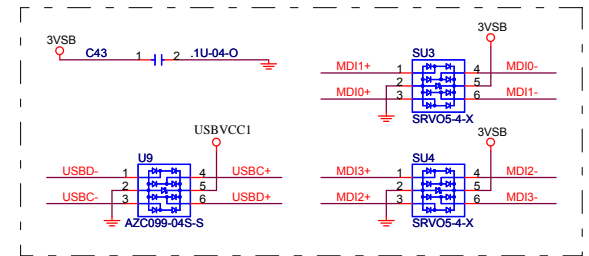
BOM Difference

	RTL8111DL-GR 1000M	RTL8102EL-GR 10/100M
Ca	RTL8111DL-GR	RTL8102EL-GR
Cb	X	V
Cc	0-04	.01U-04
Cd	X	V
Ce	V	X(LI改0805 0 ohm)
Cf	USBX2-LAN-1000	USBX2-LAN-100

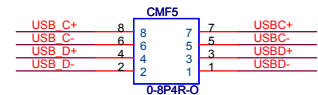
Power Difference

	RTL8111D	RTL8102E
AVDD33	3.3V	3.3V
VDD33	3VSB供應	3VSB供應
CTRL12A	Switching Output	1.2V pinself 供應
DVDD12	1.2V CTRL12A供應	1.2V pinself 供應
EVDD12	1.2V CTRL12A供應	1.2V pinself 供應

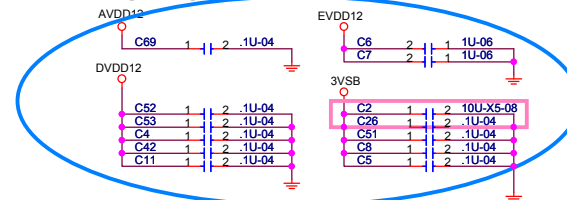
Close to connector



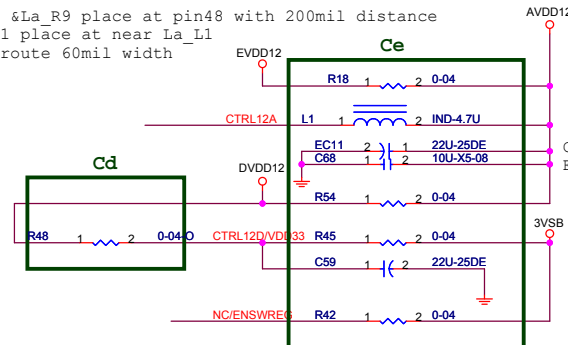
Link: Green on
Active: Yellow blinking
Link 10/100/1000: Green on
Active: Yellow blinking



close LAN1 power pin



La_L1 & La_R9 place at pin48 with 200mil distance
La_EC1 place at near La_L1
Must route 60mil width



Choke near pin48,
E/C cap near Choke

ATX P/S WITH 1A STBY CURRENT				
5VSB	5V	3.3V	12V	-12V
+/-5%	+/-5%	+/-5%	+/-5%	+/-5%

ATX4P1
12V
+/-5%

NPS08-S

VCC_DUAL

RT9214-S SW	TO252 * 2
POWER1.5V	

OP324

7.789A

ADJ1086-S

LDO

LINEAR

NPS08-S

5V_DUAL

PCI per	
5V	5.0A
3.3V	7.6A
12V	0.5A
3.3Vaux	0.375A
-12V	0.1A

X4/X1 PCIe per	
3.3V	3.0A
12V	0.5A
3.3Vaux	0.375A

X16 PCIe per	
3.3V	3.0A
12V	5.5A
3.3Vaux	0.375A

(S0 , S1 , S3 , S4 , S5)

USB X6 FR	
VDD	
5VDual	6.0A

USB X8 RL	
VDD	
5VDual	8.0A

2XPS	
5VDual	
1.0A	

3VSB

(S0 , S1 , S3 , S4 , S5)

SWITCH
UP6206

SWITCH
UP6117A

SWITCH
UP6109

(S0 , S1)

(S0 , S1)

(S0 , S1)

(S0 , S1 , S3)

Intel Havendale/Lynnfield CPU		
VCORE	VID 0.65~1.4	100A/110A
VAXG	VID 0.8~1.3	20A/25A
CPUVTT	1.1V	30/35A
VDDQ	1.5V	3/6A
VCC1_8	1.8V	1.1/1.35A

DDR3 2DIMMs		
V_DIMM	1.5V	7.2A
DDR_VTT	0.75V	0.83A

Intel PCH		
VCCDMI	1.1V	0.065A
V_CPU_IO	1.05/1.1V	<1mA
VCC_CORE	1.05V	1.629A
VCCIO	1.05V	3.251A
VCCLAN	1.05V	0.372A
VCCADPLLA	1.05V	0.075A
VCCADPLLB	1.05V	0.075A
VCCME	1.05V	2.222A
VCCACLK	1.05V	0.052A
VCCAPLLEXP	1.05V	0.045A
VCCFDIPLL	1.05V	0.037A
VCCSATAPLL	1.05V	0.031A
VCCVRM	1.8V	0.043A
VCCPNAND	1.8V	0.156A
VCCME3_3	3.3V	0.086A
VCCADAC	3.3V	0.069A
VCC3	3.3V	0.357A
VCCSUS3_3	3.3V	0.168A
VCCSUSHDA	3.3V	0.006A
RTCACC	3.3V	0.002A

FANS		
V12s0	12V	200mA

CLK GEN		
VDD*	3.3V	10mA

DVI		
V3.3s0	3.3V	180mA

USB2.0		
V5Sdual	5V	0.5A*10

SPI		
VCC	5V	10mA

AZALIA		
DVDD	3.3V	0.3A
AVDD	5V	0.1A


LAN		
VDD33	3.3V	58mA
VDD12	5V	289mA

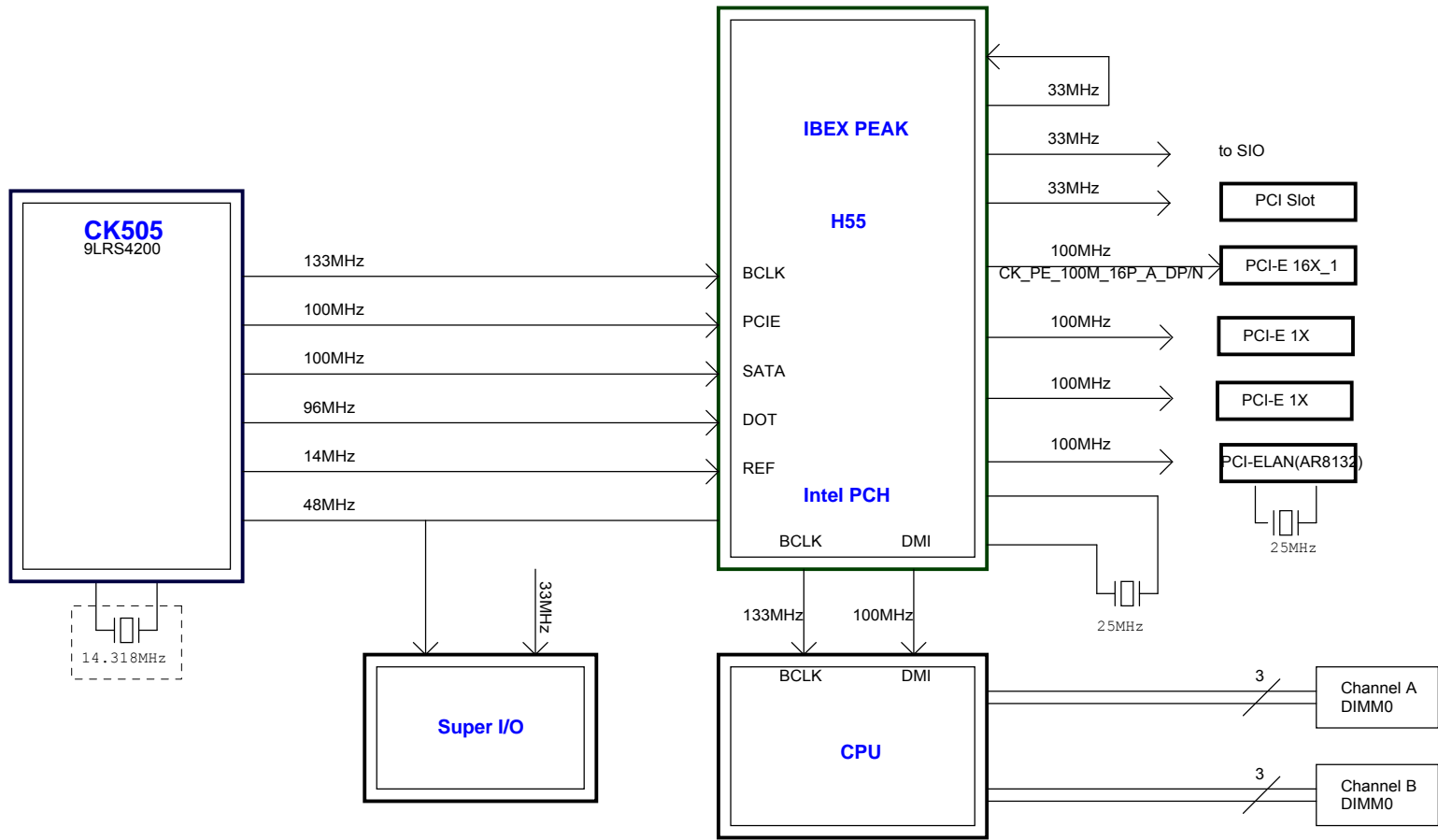
Internal VccVRM SWITCH

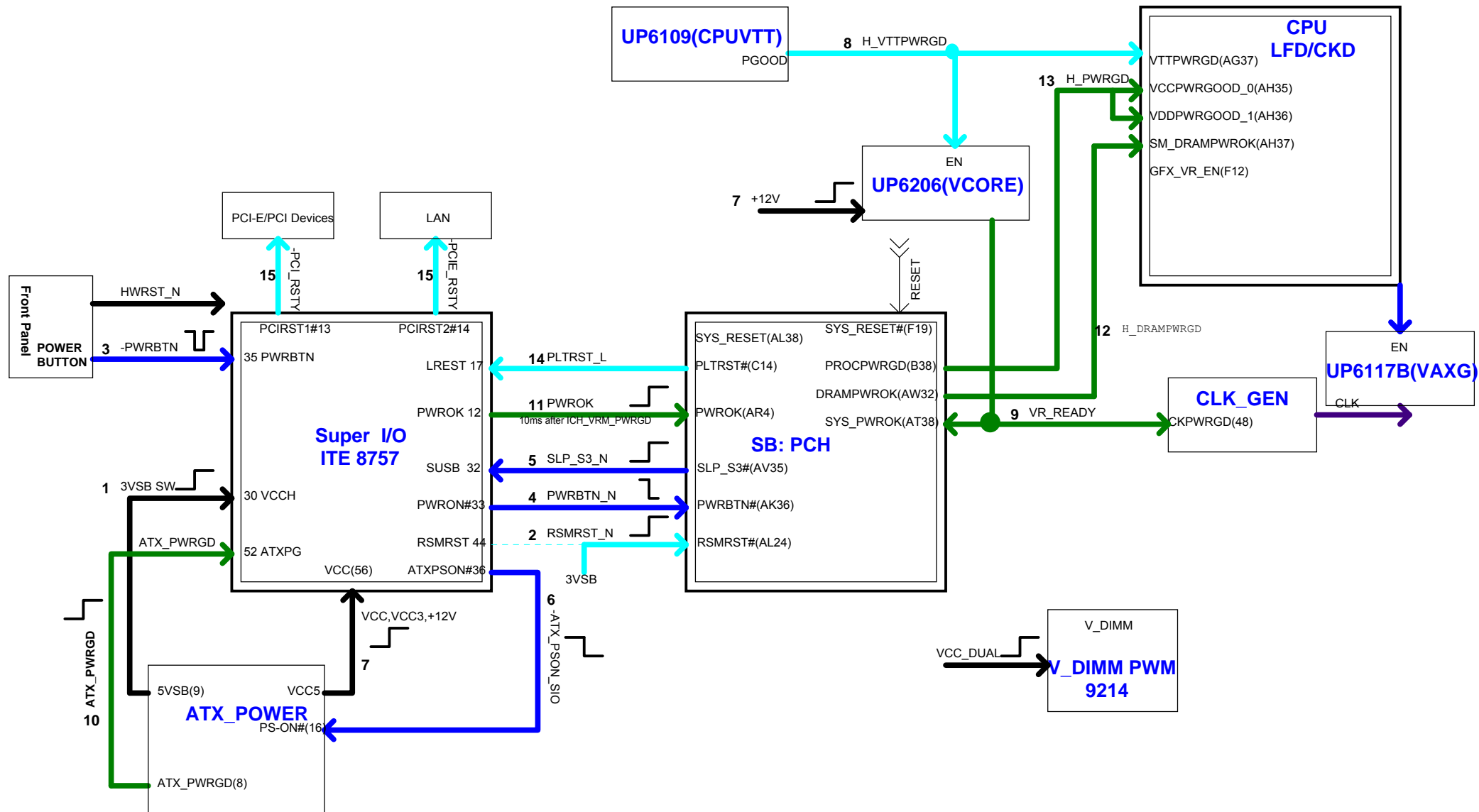
RTCVCC

BATTERY

SUPER I/O ITE8720		
5VSB	5V	15mA
VCC	5V	60mA
BAT 3.3V	3.3V	2uA
VCC3	3.3V	

 Elitegroup Computer Systems		
Title	Power Delivery Chart	
Size	Document Number	Rev
Custom	H55H-I	1.0A
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PCH STRAPS TABLE																
	H	L	DESCRIPTION	Default												
PGNT-3	(inter pu)	*Top Boot Block(-O)	A16 SWAP OVERRIDE Low: OVERRIDE	TestPoint												
PGNT-1, PGNT-0	<table><tr><td>BOOT DEVICE</td><td>GNT0</td><td>GNT1</td></tr><tr><td>LPC</td><td>0</td><td>0</td></tr><tr><td>PCI</td><td>0</td><td>1</td></tr><tr><td>*SPI</td><td>1</td><td>1</td></tr></table>		BOOT DEVICE	GNT0	GNT1	LPC	0	0	PCI	0	1	*SPI	1	1	Inter Pu Hi	SPI
BOOT DEVICE	GNT0	GNT1														
LPC	0	0														
PCI	0	1														
*SPI	1	1														
PGNT-2	(inter pu)	*(-O),Desktop not pull low	DMI AC Coupling Low: Full Voltage Mode	TestPoint												
HDA_SDO	*POWERED BY EPW(-O)	POWERED BY CORE(inter pu)	NAND VCCQ PWR WELL SEL													
HDA_SYNC	*1.5V(-O)	1.8V	OD PLL VR SUPPLY SEL													
SPI_MOSI	*EN(-O)	DIS(inter pu)	TPM FUNCTIONALITY TPM DISABLED WHEN SAMPLED LOW													
NVR_ALE	*(10K)		DANBURY Technology Enable Enable When Sampled High													
NVR_CLE	*(-O)		DMI Termination Voltage DC Coup: TX/RX To VCC Is Sampled High													
INIT3_3V_N		*(-O)	Configurable CPU Output, Stronger If Low													
SPKR	*EN(1K)	DIS	STUFF TO ENABLE NO-REBOOT OPTION AT POWER-UP (CONFIGURATION STRAPPING).													
PCH_INTVRMEN	*EN(390K)		ENABLE INTERGRATED 1.05V SUS VRM.													
PCH_PU_GP33																
IGC_EN_N		*EN	INTEGRATED CLOCK CHIP ENABLE, Stuff Low For Full Clock Integration Enable.													
VCCVRM_EN	*EN(inter pu)	DIS(-O)	OD PLL VR(VccCLK,Vccap11EXP, VccFDIPLL,VccSATAPLL; DG P383)													
PCH_GP15	*EN(10K)	DIS	INTEL ME CRYPTO TRANSPORT LAYER SECURITY (TLS) WITH CONFIDENTIALITY													

PCI ROUTING

PCI1	AD17	INTA, B, C, D	PREQ-1	PGNT-0
------	------	---------------	--------	--------

FAN_TAC1	CPU_FAN
FAN_CTL1	CPU_FAN
TMPIN1	SYS_Temp
VIN0	VCORE
VIN1	V_DIMM